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10/665,757	09/19/2003	Glenn J. Leedy	ELM-1 Cont. 9	6828

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,757	LEEDY, GLENN J.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *156-424 and 427-522* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *156-424 and 427-522* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 19 September 2003. Claims 156-424 and 427-522 are pending; claims 425 and 426 are cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 156, 157, 160, 164, 165, 167, 169, 172, 174, 175, 177, 179, 182, 184, 185, 187, 220, 222, 223, 225, 229, 231, 232, 234, 236, 238, 239, 241, 245, 247, 248, 250, 252, 292, 295, 297, 299, 329, 322, 334, 335, 337, 342, 346, 348, 349, 351, 356, 360, 361, 363, 365, 405, 409, 411, 413, 419, 421, 423, 427, 433 and 437 are rejected under 35 U.S.C. 102(b) as being anticipated by Mauger (4,966,663) ("Mauger '663").

Referring to claims 156, 165, 167, 169, 175, 177, 179, 185, 187, 220, 223, 234, 239, 245, 292, 299, 329, 335, 337, 342, 349 & 356, Mauger '663 discloses a method of making an integrated circuit where a substrate (10) has a principal surface; forming circuit devices/circuitry/active devices on the principal surface (col. 1, lines 12-20); and forming an elastic low stress/stress-controlled dielectric membrane/layer (12) overlying the circuit devices (col. 4, lines 6-24). Mauger '663 further discloses the integrated

circuit able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 9-24).

Although Mauger "663 does not specifically disclose forming the low stress membrane over the circuitry, it is inherent because the membrane is used as a mask layer (col. 1, lines 12-20).

Referring to claims 157, 160, 172, 182, 229, 232, 236, 248, 295, 332, 346, 361 & 405, Mauger '663 discloses the elastic low stress/stress-controlled dielectric membrane comprising at least one or more elastic low stress/stress-controlled dielectric layers/films (col. 5, lines 37-56).

Referring to claims 164, 174, 184, 222, 238, 250, 297, 334, 348 & 363, Mauger '663 discloses the substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate (co. 4, lines 6-10).

Referring to claims 225, 231, 241, 247, 252, 351, 360 & 365, Mauger '663 discloses removing the major portion of the substrate is removed after forming the circuitry (col. 1, lines 12-19).

Referring to claims 409, 411, 413, 419, 421, 423, 427, 433 & 437, Mauger '663 discloses the elastic low stress/stress-controlled dielectric membrane/layers are formed from at least one of an inorganic dielectric material and an organic dielectric material (abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 158, 159, 162, 163, 170, 171, 180, 181, 224, 227, 228, 230, 240, 243, 244, 246, 251, 254, 255, 267, 269, 272, 275, 278, 287, 290, 293, 294, 330, 331, 343, 344, 350, 357-359, 364, 406, 407, 452, 457, 462, 475, 480, 485, 490, 503, 508 and 513 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Mauger et al. (4,919,749) ("Mauger '749").

Mauger '663 discloses the subject matter claimed above except a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

Mauger '749 discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (12) overlying the principal surface (col. 4, lines 20-38). Mauger '749 further discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 38-58).

Referring to claims 158, 162, 170, 180, 227, 243, 254, 267, 269, 272, 275, 278, 287, 290, 293, 330, 343, 357 & 406, Mauger '749 discloses a stress of at least one of

about 0.5 to 3 x 10^8 dynes/cm^2 resulting in 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers (col. 4,lines 27-30).

Since Mauger '663 and Mauger '749 are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Mauger '749 would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by having a stress of at least one of about o.5 to 3 x 10^8 dynes/cm^2 resulting in 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers as taught by Mauger '749 for high resolution and how distortion (col. 3, lines 6-15).

Referring to claims 159, 163, 171, 181, 228, 244, 255, 294, 331, 344, 358 & 407, Mauger '663 discloses wherein the stress is tensile (col. 6, lines 51 & 52).

Referring to claims 224, 230, 240, 246, 251, 350, 359, & 364, Mauger '749 discloses removing the major portion of the substrate prior to forming the circuitry (col. 3, lines 6-14).

Referring to claims 452, 457, 462, 475, 480, 485, 490, 503, 508 and 513, Mauger '663 does not disclose forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C. It would have been obvious to one having ordinary skill in the art at the time invention was made to forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C disclosed in the claimed invention, since it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 161, 173, 183, 233, 237, 249, 268, 271, 274, 277, 286, 289, 296, 302, 333, 347, 362, 408, 410, 412, 414, 420, 422, 424, 428, 434, 436, 438, 442-445, 449, 451, 454, 456, 459, 461, 472, 474, 477, 479, 482, 484, 487, 489, 500, 502, 505, 507, 510 and 512 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Leedy (4,924,589).

Mauger '663 disclose the subject matter claimed above except depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

Leedy discloses a method of making an integrated circuit where a substrate (101) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (104) overlying the principal surface (col. 6, lines 55-68).

Referring to claims 161, 173, 183, 233, 237, 249, 296, 333, 347, 362 & 408, Leedy discloses depositing at least one of the one or more of the stress-controlled dielectric films using Chemical Vapor Deposition (col. 6, lines 65-68).

Since Mauger '663 and Leedy are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Leedy would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify

Mauger '663 by depositing at least one of the one or more of the stress-controlled dielectric films using Chemical Vapor Deposition as taught by Leedy to prevent defects (col. 2, lines 1-12).

Referring to claims 268, 271, 274, 286, 289, 302, 442-445, 451, 456, 461, 474, 479, 484, 489, 502, 507, 512, Leedy discloses the at least one or more elastic low stress/stress-controlled dielectric membrane/layer to be at least one of elastic and substantially flexible (col. 6, line 68 thru col. 7, line 5).

Referring to claims 410, 412, 414, 420, 422, 424, 428, 434, 436 & 438, Leedy discloses the elastic low stress/stress-controlled dielectric membrane/layers are formed from at least one of an inorganic dielectric material and an organic dielectric material, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride (col. 6, lines 65-68).

Referring to claims 449, 454, 459, 472, 477, 482, 487, 500, 505 &510, Leedy discloses at least one flexible integrated circuit overlying the integrated circuit (col. 2, lines 24-33).

Claims 166, 168, 176, 178, 186, 188, 221, 226, 235, 242, 253, 298, 300, 336, 338, 345, 352, and 366 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Shimizu et al. (4,618,397).

Mauger '663 discloses the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44).

Referring to claims 166, 168, 176, 178, 186, 188, 221, 226, 235, 242, 253, 298, 300, 336, 338, 345, 352, & 366, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Mauger '663 and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimitzu et al. would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 189, 192, 194, 196, 207-212, 256-261, 265, 266, 305, 306, 310, 312, 314, 320-322, 325, 340, 341, 354, 355, 367, 368, 370, 373, 375, 377, 380, 381, 415. 429, 431, 439, 448, 453, 458, 466, 471, 476, 481, 486, 494, 498, 499, 504, 509 and 517 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stein (4,070,230).

Mauger '663 discloses the subject matter claimed above except transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

Referring to claims 189, 194, 196, 314, 322, 370, 375, 377, 448, 453, 458, 471, 476, 481, 486, 499, 504 & 509, Stein discloses a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuit devices/circuitry/active devices (8) on the principal surface; and forming a layer (9) overlying the circuit devices (8) (col. 4, lines 27-55). Stein further discloses the integrated circuit able to have a major portion of the substrate (1) removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 7-24). Stein also discloses transferring information through interconnections formed passing through the layer, wherein the interconnections are at least one of electrical and optical interconnections (col. 5, lines 32-41).

Since Mauger '663 and Stein are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stein would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by transferring information through interconnections formed passing through the layer as taught by Stein to prevent defects (col. 1, lines 22-48).

Referring to claims 192, 310, 325, 373, Mauger '663 discloses the elastic low stress/stress-controlled dielectric membrane comprising at least one or more elastic low stress/stress-controlled dielectric layers/films.

Referring to claims 207, 209, 211, 256, 258, 260, 265, 305, 320, 340, 354, 367 & 380, Stein discloses providing a second integrated circuit overlying the integrated circuit; and providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit (col. 8, lines 26-34).

Referring to claims 208, 210, 212, 257, 259, 261, 266, 306, 321, 341, 355, 368 & 381, Stein discloses providing a plurality of integrated circuits overlying the integrated circuit; and providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit (col. 8, lines 26-34).

Referring to claims 312, Mauger '663 discloses the substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

Referring to claims 415, 429, 431 & 439, Mauger '663 discloses the elastic low stress/stress-controlled dielectric membrane/layers are formed from at least one of an inorganic dielectric material and an organic dielectric material.

Referring to claims 466, 494, 498 and 517, Mauger '663 does not disclose forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400^{o}C. It would have been obvious to one having ordinary skill in the art at the time invention was made to forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400^{o}C disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 190, 191, 308, 309, 318, 323, 324, 328, 371 and 372 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stein as applied to claims 189, 307, 322 and 370 above, and further in view of Mauger '749.

Mauger '663 in view of Stein disclose the subject matter claimed above except a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

Mauger '749 discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (12) overlying the principal surface (col. 4, lines 20-38). Mauger '749 further discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 38-58).

Referring to claims 190, 281, 308, 318, 323, 328 & 371, Mauger '749 discloses a stress of at least one of about 0.50to 3×10^8 dynes/cm^2 resulting in 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers (col. 4, lines 27-30).

Since Mauger '663 and Mauger '749 are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Mauger '749 would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by having a stress of at least one of about 0.5 to 3×10^8 dynes/cm^2

resulting in 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers as taught by Mauger '749 for high resolution and how distortion (col. 3, lines 6-15).

Referring to claims 191, 309, 324, & 372, Mauger '663 discloses wherein the stress is tensile (col. 6, lines 51 &52).

Claims 193, 280, 311, 317, 326, 327, 374, 416, 430, 432, 440, 446, 463, 465, 491, 493, 495, 497, 514 and 516 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stein as applied to claims 189, 307, 322 and 370 above, and further in view of Leedy.

Mauger '663 in view of Stein disclose the subject matter claimed above except depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

Leedy discloses a method of making an integrated circuit where a substrate (101) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (104) overlying the principal surface (col. 6, lines 55-68).

Referring to claims 193, 311, 326 & 374, Leedy discloses depositing at least one of the one or more of the stress-controlled dielectric films using Chemical Vapor Deposition (col. 6, lines 65-68).

Since Mauger '663 and Leedy are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Leedy would have

been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by depositing at least one of the one or more of the stress-controlled dielectric films using Chemical Vapor Deposition as taught by Leedy to prevent defects (col. 2, lines 1-12).

Referring to claims 280, 317, 327 & 446, 465 493, 497, 516, Leedy discloses the at least one or more elastic low stress/stress-controlled dielectric membrane/layer to be at least one of elastic membrane and substantially flexible membrane (col. 6, lines 68 thru col. 7, line 5).

Referring to claims 416, 430, 432 & 440, Leedy discloses the elastic low stress/stress-controlled dielectric membrane/layers are formed from at least one of an inorganic dielectric material and an organic dielectric material, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride (col. 6, lines 65-68).

Referring to claims 463, 491, 495, 514, Leedy discloses at least one flexible integrated circuit overlying the integrated circuit (col. 2, lines 24-33).

Claims 195, 107, 313, 315, 376 and 378 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stein as applied to claims 189, 307 and 370 above, and further in view of Shimizu et al.

Mauger '663 in view of Stein disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44).

Referring to claims 195, 197, 313, 315, 376 & 378, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity.

Since Mauger '663 and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimitzu et al. would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 198, 201, 203, 205, 382, 385, 387, 389, 417 and 441 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. (4,835,765).

Mauger '663 discloses the subject matter claimed above except an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and transferring a plurality of data bytes between the data source and data sink of an interconnect circuitry of the integrated circuit.

Referring to claims 198 & 382, Bergmans et al. disclose a method of using an integrated circuit having a data source (7) formed on a first portion of the integrated circuit (1), a data sink (13) formed on a second portion of the integrated circuit (1), interconnect circuitry interconnecting the data source (7) and the data sink (13); transferring a plurality of data bytes between the data source (7) and data sink (13) of the interconnect circuitry of the integrated circuit (1) (col. 3, lines 30-51).

Since Mauger '663 and Bergmans et al. are both from the same field of endeavor, a method of using an integrated circuit, the purpose disclosed by Bergmans et al. '663 would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by having an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and transferring a plurality of data bytes between the data source and data sink of an interconnect circuitry of the integrated circuit as taught by Bergmans et al. to reduce defects (col. 3, lines 52-64).

Referring to claims 201 & 385, Mauger '663 discloses the elastic low stress/stress-controlled dielectric membrane comprising at least one or more elastic low stress/stress-controlled dielectric layers/films (col. 5, lines 37-56).

Referring to claims 203, 205, 387 & 389, Mauger '663 discloses the integrated circuit able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 37-56).

Referring to claims 417 & 441, Mauger '663 discloses the elastic low stress/stress-controlled dielectric membrane/layers are formed from at least one of an inorganic dielectric material and an organic dielectric material (abstract).

Referring to claims 470 and 522, Mauger '663 does not disclose forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400^{o}C. It would have been obvious to one having ordinary skill in the art at the time invention was made to forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400^{o}C disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 199, 200, 284, 383 and 384 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. as applied to claims 198 and 382 above, and further in view of Mauger '749.

Mauger '663 in view of Bergmans et al. disclose the subject matter claimed above except a stress of at least one of about 8 x 10^{8} dynes/cm^{2} or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

Mauger '749 discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (12) overlying the principal surface (col. 4, lines 20-

38). Mauger '749 further discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 38-58).

Referring to claims 199 & 383, Mauger '749 discloses a stress of at least one of about 0.5 to 3 x 10^8 dynes/cm^2 resulting in 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers (col. 4, lines 27-30).

Since Mauger '663 and Mauger '749 are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Mauger '749 would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by having a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers as taught by Mauger '749 for high resolution and how distortion (col. 3, lines 6-15).

Referring to claims 200 & 384, Mauger '663 discloses wherein the stress is tensile (col. 6, lines 51 &52).

Claims 202, 283, 386, 418, 442, 447, 467, 519 and 521 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. as applied to claims 198 and 382 above, and further in view of Leedy.

Mauger '663 in view of Bergmans et al. disclose the subject matter claimed above except depositing at least one of the one or more of the stress-controlled

dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

Leedy discloses a method of making an integrated circuit where a substrate (101) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (104) overlying the principal surface (col. 6, lines 55-68).

Referring to claims 202 & 386, Leedy discloses depositing at least one of the one or more of the stress-controlled dielectric films using Chemical Vapor Deposition (col. 6, lines 65-68).

Since Mauger '663 and Leedy are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Leedy would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by depositing at least one of the one or more of the stress-controlled dielectric films using Chemical Vapor Deposition as taught by Leedy to prevent defects (col. 2, lines 1-12).

Referring to claims 283, 447, 469 & 521, Leedy discloses the at least one or more elastic low stress/stress-controlled dielectric membrane/layer to be at least one of elastic membrane and substantially flexible membrane (col. 6, line 68 thru col. 7, line 5).

Referring to claims 418 & 442, Leedy discloses the elastic low stress/stress-controlled dielectric membrane/layers are formed from at least one of an inorganic dielectric material and an organic dielectric material, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride (col. 6, lines 65-68).

Referring to claims 467 & 519, Leedy discloses at least one flexible integrated circuit overlying the integrated circuit (col. 2, lines 24-33).

Claims 204, 206, 388 and 390 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. as applied to claims 198 and 382 above, and further in view of Shimizu et al.

Mauger '663 in view of Bergmans et al. disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, liens 29-44).

Referring to claims 204, 206, 388 & 390, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity.

Since Mauger '663 and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimitzu et al. would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 213, 214, 392 and 393 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. as applied to claims 198 and 382 above, and further in view of Stein.

Mauger '663 in view of Bergmans et al. disclose the subject matter claimed above except providing a plurality of integrated circuits overlying the integrated circuit; and providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

Stein discloses a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuit devices/circuitry/active devices (8) on the principal surface; and forming a layer (9) overlying the circuit devices (col. 4, lines 27-55). Stein further discloses the integrated circuit able to have a major portion of the substrate (1) removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 7-24). Stein also discloses transferring information through interconnections formed passing through the layer, wherein the interconnections are at least one of electrical and optical interconnections (col. 5, lines 32-41).

Referring to claims 213, 392 & 518, Stein discloses providing a second integrated circuit overlying the integrated circuit; and providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit (col. 8, lines 26-34).

Referring to claims 214 & 393, Stein discloses providing a plurality of integrated circuits overlying the integrated circuit; and providing at least one interconnect that

connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit (col. 8, lines 26-34).

Since Mauger '663 and Stein are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stein would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by providing a plurality of integrated circuits overlying the integrated circuit; and providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit as taught by Stein to prevent defects (col. 1, lines 22-48).

Claims 215-217, 262-264, 270, 273, 276, 279, 288, 291, 301, 339, 353 and 369 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Mauger '749 as applied to claims 156, 169, 179, 220, 234, 245, 292, 329, 342 and 356 above, and further in view of Shimizu et al.

Mauger '663 in view of Mauger '749 disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, liens 29-44).

Referring to claims 215-217, 262-264, 270, 273, 276, 279, 288, 291, 301, 339 & 369, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity (col. 1, liens 45-56).

Since Mauger '663 and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimitzu et al. would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 218, 282, 316, 319 and 379 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stein and Mauger '749 as applied to claims 189, 307, 322 and 370 above, and further in view of Shimizu et al.

Mauger '663 in view of Stein and Mauger '749 disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, liens 29-44).

Referring to claims 218, 282, 316, 319 & 379, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Mauger '663 and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimitzu et al. would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 219, 285 and 391 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. and Mauger '749 as applied to claims 198 and 382 above, and further in view of Shimizu et al.

Mauger '663 in view of Bergmans et al. and Mauger '749 disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, liens 29-44).

Referring to claims 219, 285 & 391, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Mauger '663 and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimitzu et al. would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being able to be thinned to about 25 microns or less throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claim 304 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Mauger '749 and Shimizu et al. as applied to claim 292 above, and further in view of Leedy.

Mauger '663 in view of Mauger '749 and Shimizu et al. disclose the subject matter claimed above except at least one or more elastic low stress/stress-controlled dielectric membrane/layer to be at least one of elastic and substantially flexible.

Leedy discloses a method of making an integrated circuit where a substrate (101) has a principal surface; and forming an elastic low stress/stress-controlled dielectric membrane/layer (104) overlying the principal surface (col. 6, lines 55-68).

Referring to claim 304, Leedy discloses the at least one or more elastic low stress/stress-controlled dielectric membrane/layer to be at least one of elastic and substantially flexible (col. 6, line 68 thru col. 7, line 5).

Since Mauger '663 and Leedy are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Leedy would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by at least one or more elastic low stress/stress-controlled dielectric membrane/layer to be at least one of elastic and substantially flexible as taught by Leedy to prevent defects (col. 2, lines 1-12).

Claim 303 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Mauger '749 as applied to claim 292 above, and further in view of Stevenson.

Mauger '663 in view of Mauger '749 disclose the subject matter claimed above except the integrated circuit is be at least one of elastic and substantially flexible.

Stevenson discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming a dielectric membrane/layer (18) overlying the principal surface (col. 4, lines 10 &11). Stevenson discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 12-23).

Referring to claims 303, Stevenson discloses the integrated circuit is at least one of elastic and substantially flexible (col. 1, lines 19-30).

Since Mauger '663 and Stevenson are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stevenson would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by the integrated circuit being at least one of elastic and substantially flexible by Stevenson to serve as an etch-stop layer thereby achieving a smooth etched surface (col. 2, lines 20-39).

Claims 394, 450, 455, 460, 473, 478, 483, 488, 501, 506 and 511 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stevenson (4,721,938).

Mauger '663 discloses the subject matter claimed above except forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

Stevenson discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming a dielectric membrane/layer (18) overlying the principal surface (col. 4, lines 10 &11). Stevenson discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 12-23).

Referring to claims 394-400, 402-404, Stevenson discloses forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer (12) (col. 4,lines 28-31).

Since Mauger '663 and Stevenson are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stevenson would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer as taught by Stevenson to serve as an etch-stop layer thereby achieving a smooth etched surface (col. 2, lines 20-39).

Referring to claims 450, 455, 460, 473, 478, 483, 488, 501, 506 & 511, Stevenson discloses the integrated circuit as at least one of a substantially flexible integrated circuit and an elastic integrated circuit (col. 1, lines 19-30).

Claims 401, 464 492, 496, & 515 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Stein as applied to claim 307 above, and further in view of Stevenson.

Mauger '663 in view of Stein disclose the subject matter claimed above except forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

Stevenson discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming a dielectric membrane/layer (18) overlying the principal surface (col. 4, lines 10 &11). Stevenson discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 12-23).

Referring to claim 401, Stevenson discloses forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer (12) (col. 4,lines 28-31).

Since Mauger '663 and Stevenson are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stevenson would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer as taught by Stevenson to serve as an etch-stop layer thereby achieving a smooth etched surface (col. 2, lines 20-39).

Referring to claims 464 492, 496, & 515, Stevenson discloses the integrated circuit as at least one of a substantially flexible integrated circuit and an elastic integrated circuit (col. 1, lines 19-30).

Claims 468 and 520 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mauger '663 in view of Bergmans et al. as applied to claim 307 above, and further in view of Stevenson.

Mauger '663 in view of Bergmans et al. disclose the subject matter claimed above except the integrated circuit as at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

Stevenson discloses a method of making an integrated circuit where a substrate (10) has a principal surface; and forming a dielectric membrane/layer (18) overlying the principal surface (col. 4, lines 10 &11). Stevenson discloses the integrated circuit able to have a major portion of the substrate (10) removed throughout a full extent thereof while retaining its structural integrity (col. 4, lines 12-23).

Referring to claims 468 & 520, Stevenson discloses the integrated circuit as at least one of a substantially flexible integrated circuit and an elastic integrated circuit (col. 1, lines 19-30).

Since Mauger '663 and Stevenson are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stevenson would have been recognized in the pertinent art of Mauger '663. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mauger '663 by having the integrated circuit as at least one of a substantially flexible integrated circuit and an elastic integrated circuit as taught by Stevenson to serve as an etch-stop layer thereby achieving a smooth etched surface (col. 2, lines 20-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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